UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/444,675	11/22/1999	TORU KOIZUMI	35.C14029	8958

5514 7590 11/21/2003

FITZPATRICK CELLA HARPER & SCINTO
30 ROCKEFELLER PLAZA
NEW YORK, NY 10112

EXAMINER	
WU, DOROTHY	

ART UNIT	PAPER NUMBER
2615	8

DATE MAILED: 11/21/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/444,675	KOIZUMI ET AL.	
	Examiner	Art Unit	
	Dorothy Wu	2615	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-20 is/are pending in the application.

4a) Of the above claim(s) 10-20 is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-9 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 5 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election/Restrictions

1. Applicant's election of Group I in Paper No. 7 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 6 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claim 6, the claim recites the limitation "the pixel has a charge/voltage conversion unit and is connected to said buried photodiode through a transfer switch." It is unclear whether the pixel or the charge/voltage conversion unit is connected to the buried photodiode.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are

such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 5, 7, and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art in view of Vu et al, U.S. Patent 6,025,875.

Regarding claim 1, the admitted prior art teaches a sensor integrated on a single semiconductor substrate (page 1, lines 10-12) comprising a sensor block including a pixel unit comprising a plurality of pixels each including a light-receiving element and a scanning unit for selecting a pixel of said pixel unit (page 1, lines 12-15) and a signal processing block for processing a signal output from said sensor block (page 1, lines 16-18). The admitted prior art does not teach that the power supply voltage or an amplitude or high level of a clock signal used in said sensor block is higher than a power supply voltage of said signal processing block. Vu teaches that the power voltage of a signal processor is lower than the voltage of a CCD or CIS image sensor (col. 4, lines 6-13). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the process of fabricating the sensor block and signal processing block on a single substrate as taught by the admitted prior art with the practice of using a lower voltage supply for the signal processing block than for the sensor block taught by Vu to make a sensor with the pixel units and signal processing units on the same substrate, wherein the power supply for the signal processing unit is lower than the power supply for the imager. One of ordinary skill would have been motivated to make such a modification to reduce the time needed to transfer data from one functional unit to another by integrating the units on the same substrate, thus shortening the path between the units, and to reduce the overall power consumption of the sensor by operating units at a lower power supply.

Regarding claim 5, the admitted prior art teaches that the light-receiving element is a buried photodiode (page 2, line 5).

Regarding claim 7, Vu teaches that the sensor block and signal processing block are connected via level shift means (coupling capacitor C_{CL}) for shifting a signal level (col. 4, lines 9-13).

Regarding claim 8, the admitted prior art teaches that a conventional image sensing apparatus has a data processing system for A/D converting the signal (page 2, lines 21, 24-27). It would have been obvious to one of ordinary skill to incorporate the A/D conversion into the signal processing block.

4. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art in view of Vu et al, U.S. Patent 6,025,875, and further in view of Mann et al, U.S. Patent 6,121,087.

Regarding claim 2, the admitted prior art in view of Vu teach the apparatus of claim 1. See above. The admitted prior art in view of Vu do not teach that a gate insulating layer of at least some insulated gate transistors of said sensor block is thicker than that of an insulated gate transistor used in said signal processing block. Mann et al teaches that the application of a higher voltage will require a thicker gate oxide layer to prevent oxide breakdown (col. 6, lines 34-42). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the practice of growing a thicker oxide when a higher voltage is being applied taught by Mann into the apparatus of the admitted prior art in view of Vu to make an image sensing apparatus that uses a higher power voltage, and thus thicker gate oxide layers, for

the sensor block and a lower power voltage, and thus thinner gate oxide layers, for the signal processing block. One of ordinary skill would have been motivated to make such a modification to fabricate the appropriate thickness of oxide for the voltage that shall be used upon it.

5. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art in view of Vu et al, U.S. Patent 6,025,875, in view of Mann et al, U.S. Patent 6,121,087, and further in view of Gardner et al, U.S. Pub. No. 2002/0022325.

Regarding claim 4, the admitted prior art in view of Vu teach the apparatus of claim 1. See above. The admitted prior art in view of Vu in view of Mann teach that the gate insulating layers of some transistors of said sensor block is thicker than that of an insulated gate transistor used in said signal processing block. See above. The admitted prior art in view of Vu in view of Mann do not teach that a threshold voltage of at least some insulated gate transistors of said sensor block is higher than that of an insulated gate transistor used in said signal processing block. Gardner teaches that thinner gate oxides will require a lower threshold voltage [0008]. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teaching of having a lower threshold voltage when a transistor has a thinner gate oxide taught by Gardner into the apparatus of the admitted prior art in view of Vu in view of Mann to make an image sensing apparatus whose transistors in the signal processing block use a lower power supply and possess a lower threshold voltage than the transistors on the signal processing block. One of ordinary skill would have been motivated to make such a modification to reduce the power consumption of the sensor block by using different power

supplies and reduce the fabrication time by growing thinner oxides that require lower threshold voltages.

6. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art in view of Vu et al, U.S. Patent 6,025,875, in view of Mann et al, U.S. Patent 6,121,087, and further in view of Sawada et al, U.S. Patent 6,184,516.

Regarding claim 3, the admitted prior art in view of Vu teaches the apparatus of claim 1. See above. The admitted prior art in view of Vu in view of Mann teach that the threshold voltages for the sensor block transistors are higher than the threshold voltages for the signal processing block transistors. See above. The admitted prior art in view of Vu in view of Mann do not teach that the well density of at least some insulated gate transistors of said sensor block is lower than that of an insulated gate transistor used in said signal processing block. Sawada teaches a pMOS transistor 323 is formed on an n type well 19 whose impurity concentration is higher than that of the n type semiconductor substrate on which the n type well 19 is formed, and a pMOS transistor 324 is formed outside of the n type well 19 on the n type semiconductor substrate. The threshold voltage of pMOS transistor 323 formed on the n type well 19 is about -0.75 V, and that the threshold voltage of the pMOS transistor 324 formed outside of the n type well on the n type semiconductor substrate is about -0.29V (col. 6, lines 61-col. 7, line 8). Therefore, Sawada teaches that the transistor formed in a substrate possessing a lower well impurity concentration will have a higher threshold voltage. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of fabricating a transistor in a substrate with a lower impurity concentration to achieve a

higher threshold voltage taught by Sawada with the apparatus of the admitted prior art in view of Vu in view of Mann to make an image sensing apparatus whose signal processing block transistors use lower voltage, possess thinner gate oxide layers, and are fabricated in wells of lower impurity concentration than those of the transistors on the signal processing block. One of ordinary skill would have been motivated to make such a modification to reduce the overall power consumption of the chip.

7. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art in view of Vu et al, U.S. Patent 6,025,875, and further in view of Tandon et al, EPO 0 254 497.

As best understood from the language of the claim, regarding claim 6, the admitted prior art in view of Vu teach the apparatus of claim 5. See above. The admitted prior art in view of Vu do not teach that each pixel has a charge/voltage conversion unit connected to the buried photodiode through a transfer switch. Tandon does teach that each pixel has a charge/voltage conversion unit (source follower 33) connected to a photodiode (14) through a transfer switch (phi.1) (col. 3, lines 25-32). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the charge/voltage conversion unit and transfer switches of Tandon into the apparatus of the admitted prior art in view of Vu to make an image sensing apparatus that uses a lower power supply for the signal processing block than the sensor and converts the photoelectric charge accumulated in the pixels into voltage when the charge is transferred. One of ordinary skill would have been motivated to make such a modification to control when the charges are transferred and converted to voltages.

8. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art in view of Vu et al, U.S. Patent 6,025,875, and further in view of well-known prior art.

Regarding claim 9, the admitted prior art in view of Vu teach the apparatus of claim 8. See above. Although the admitted prior art in view of Vu do not teach a circuit for forming a luminance signal and a chrominance signal, the office takes Official Notice that it would have been obvious to one of ordinary skill in the art at the time the invention was made to separate the image data of the admitted prior art in view of Vu into luminance and chrominance signals. One of ordinary skill would have been motivated to make such a modification to convert the image data into a format that is commonly used in signal processing methods.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dorothy Wu whose telephone number is 703-305-8412. The examiner can normally be reached on Monday-Friday, 9:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Andrew Christensen can be reached on 703-308-7644.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

Or faxed to:

(703) 872-9314

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703)306-0377.

Dorothy Whitney

DW
November 13, 2003

ANDREW CHRISTENSEN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600